UCF Stands For Opportunity

UNIVERSITY OF CENTRAL FLORIDA & THE SCHOOL OF EECS

present the Spring 2009

EECS Seminar Series

Dr. Steven Voldman

IEEE Fellow, ESD Association Board of Director, ESD Standards Chairman for Transmission Line Pulse testing, and member of the Education Committee

"ESD: Failure Mechanisms — Nano Defects in the Nano Electronic Era"

Wednesday, April 15, 2009 • 11:00 a.m. • Harris Center (HEC) 101

ESD failure mechanisms continue impact semiconductor components and systems as technologies continue to scale from micro- to nano-electronics. With the evolution and scaling of technology, ESD failure mechanisms occur in CMOS, Silicon-on-Insulator (SOI), RF CMOS, Gallium Arsenide, magnetic recording industry, smart power, micro electromechanical (MEM) structures, to photo-masks and reticles. This lecture takes a look at electrical overstress, electrostatic discharge, and latchup from a failure analysis and case-study approach. The text provides a clear insight into the physics of failure from a generalist perspective, followed by investigation of failure mechanisms in specific technologies, circuits, and systems. The lecture takes a unique twist by covering both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit methodology. This lecture will emphasize on failure analysis, electro-thermal models, and technologies; the state-of-the-art technologies discussed include CMOS, BiCMOS, Silicon on Insulator (SOI), bipolar technology, high voltage CMOS (HVCMOS), RF CMOS, smart power, Gallium Arsenide (GaAs), magneto-resistive (MR) ,giant magneto-resistors (GMR), tunneling magneto-resistor (TMR), photo-masks and reticles, to micro-electromechanical systems (MEMs). In the area of MEMs, the lecture will present the discussions on micro-motors, RF MEM switches, to micro-mirror arrays.

This lecture will be based on the future released book ESD: Failure Mechanisms and Models. This text is a continuation of the authors' series of books on electrostatic discharge (ESD) protection.; this book will be an invaluable reference in the present issues that confront modern technology as we enter the Nano-electronic Era. Its academic treatment will appeal and be illuminating to both senior and graduate students with interests in nano-electronics.

DR. STEVEN H. VOLDMAN

Dr. Steven H. Voldman is an IEEE Fellow for "Contributions in ESD protection in CMOS, Silicon On Insulator and Silicon Germanium Technology." He was the recipient of the ESD Association Outstanding Contribution Award in 2007. He received his B.S. in Eng. Science from Univ. of Buffalo (1979); a first M.S. EE (1981) from Massachusetts Institute of Technology (MIT); a second degree EE Degree (Engineer Degree) from MIT; a MS Eng. Physics (1986) and a Ph.D EE (1991) from Univ. of Vermont under IBM's Resident Study Fellow program.

He was a member of the IBM development for 25 years working on Bipolar SRAM, CMOS DRAM, CMOS logic, Silicon on Insulator (SOI), BiCMOS, Silicon Germanium (SiGe), RF CMOS, RF SOI, smart power, and image processing technology. In 2008, he was a member of the Qimonda DRAM development team, working on 70, 58 and 48 nm technology. In 2008, he worked in Hsinchu, Taiwan for Taiwan Semiconductor Manufacturing Corportion (TSMC) as part of the 45 nm ESD and latchup development team. He is presently a Senior Principal Engineer working for the Intersil Corporation on ESD and Latchup.

Dr. Voldman was chairman of the SEMATECH ESD Working Group, from 1995 to 2000. He is presently a member of the ESD Association Board of Director, ESD Standards Chairman for Transmission Line Pulse testing, and member of the Education Committee. He initiated the "ESD on Campus" program which was established to bring ESD lectures and interaction to university faculty and students internationally; the ESD on Campus program has reached over 32 universities in the United States, Singapore, Taiwan, Malaysia, Philippines, Thailand, India, and China. He is presently General Chairman for the EOS/ESD Symposium in 2009, and is a member of the technical program committee for the Taiwan ESD Symposium, and the first International Workshop on ESD (IWESD) in Hangzhou, China. Dr. Voldman has written over 150 technical papers between 1982 and 2009. He is a recipient of over 182 issued US patents and 125 US patent application, in the area of ESD and CMOS latchup. Dr. Voldman also has written an articles for Scientific American and is an author of the book series ESD: Physics and Devices, ESD:Circuits and Devices, ESD: Radio Frequency (RF) Technology and Circuits, a fourth text, Latchup, and a new fifth text, ESD: Failure Mechanisms and Models, as well as a contributor to the book Silicon Germanium: Technology, Modeling and Design.

SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

www.eecs.ucf.edu • click on "Colloquiums & Seminars"